Routing Algorithms and Performance Evaluation in Network on Chips

Ashish Rai[1], Dr. Prabhat Mathur[2]
Department of Computer Science
Lachoo Memorial College of Science & Technology
Jodhpur, India
ashishrailmc@gmail.com[1], mathur_prabhat@yahoo.com[2]

***Abstract*—The advances in semiconductor technologies have enabled the integration of all components of a complicated system on a relatively small chip. This concept is referred to as System-on-Chip (SoC). By the further downscaling of the feature size and at the same time a growing demand for more functionality, the number of IP modules on a single chip are increasing. Hence, SoCs with hundreds of IP cores are becoming a reality. As the number of IP modules in Systems-on-Chip (SoCs) increases, bus-based interconnection architectures may prevent these systems to meet the performance required by many applications. For systems with intensive parallel communication requirements buses may not provide the required bandwidth, latency, and power consumption. A solution for such a communication bottleneck is the use of an embedded switching network, called *Network-on-Chip (NoC),* to interconnect the IP modules in SoCs. This paper discusses various routing algorithms and performance parameters used in NoC.**

Keywords: NoC, Routing algorithms, System on Chips, performance evaluations.

I. INTRODUCTION

Network on Chip (NoC) is a new paradigm for System on Chip (SoC) design. Increasing integration produces a situation where bus structure, which is commonly used in SoC, becomes blocked and increased capacitance poses physical problems. In NoC architecture traditional bus structure is replaced with a network which is a lot similar to the Internet. Data communications between segments of chip are packetized and transferred through the network. The network consists of wires and routers. Processors, memories and other IP-blocks (Intellectual Property) are connected to routers. A routing algorithm plays a significant role on network□s operation. Routers make the routing decisions based on the routing algorithm. SoCs consist of various IP blocks, routers, and physical links. IP block (in some literature terms such as processing element (PE) or virtual component are also used) is a general term used for representing such entities as DSPs, memory modules, MPEG decoders, processor cores and so on.

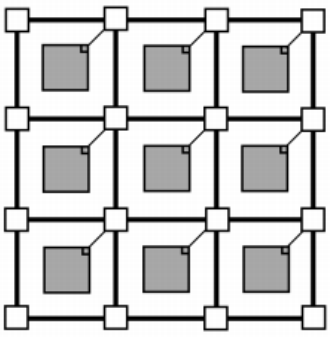

Figure 1.1 Network on Chip

Routers and links are employed for providing communication infrastructure for IP blocks in other words they organize a NoC. Routers have input and output ports which are connected to IP blocks and other routers in the system. The number of ports depends on the network topology. Physical links are actually copper wires utilized for data transmission between adjacent routers and IP blocks. The messages sent via physical links are divided into packets or flits depending on the used switching technique. Packet is a fixed length data block containing all the control and routing information, which gives the router an opportunity to decide where the incoming packet should be sent, in its header. Sometimes packets are further split into flits (flow control units). Unlike packets just

the first flit called header flit involves routing information; its main task is reserving a path for other flits (data flits) following it, the last flit is a tail flit which releases all the resources reserved by header flit.

II. RELATED WORK

Viswanathan et all[1], presented a network calculus based analytical model is used to evaluate the performance and cost metrics like end-to-end delay, buffer size and area requirement of the 3D RNT. The arrival and service curve of a switch of the 3D topology is derived from which the delay and input buffer size of the switch can be computed easily for a given traffic pattern. The end-to-end delay of the five data flows are computed by summing up the delay bound of the switches participating in the data flows. Further, input buffer size of the switches participating in the data flows are computed and discussed on the influence of the switch buffer size in determining the area overhead requirement under various injection rate and burst size of the data. Simulation also carried out using an open source simulator NS-2 to validate the effectiveness of the model. The performance and cost metrics deviation is about 14 % between the model and the simulation. The methodology used in the paper can provide the designers an intricate insight on the influence of the traffic related parameters in determining the performance and area requirement of a 3D NoC topology which is useful as far as the design space of the 3D NoC architecture is concerned.

Andreas Hanemann et all[2] presented some results of a study for harmonising the choice of network performance metrics in a multi-domain environment, and for defining common procedures for metric post-processing (or composition). In particular, they classified the possible compositions in three main categories: aggregation in time, aggregation in space, concatenation in space, and explained the utility and challenges associated with each of them. For concatenation in space, we also presented the analysis of some One Way Delay data we collected, the analysis being finalised to validate a procedure for getting a picture of the performances on an end-to-end path given the availability of performance measurements only on disjoint sections of the path. This operation has an important practical utility, since in large network it is unpractical to setup dedicated measurements among each possible couple of end points of interest.

Salem NASRI [3] studies the NoC switcher modelling with network calculus theory. It presents a model providing the bounds for network delay and buffering requirements. The main goal of this work was a contribution to network flow modeling with theoretical approach. As a result, a model for network delay is developed. It contributes on the QoS evaluation and NoC management in where critical time applications are enhanced. This work has completed with a study and development of a QoS model of multi application systems with multi parameters. This helps to make up the efficiency of the QoS metric evaluation.

Umit Y. Ogras and Radu Marculescu[4] presented a novel router model for NoC performance analysis. This approach provides not only aggregate performance metrics such as average latency and throughput, but also feedback about the network characteristics (e.g., buffer utilization, average latency per router and per flow) at a fine-level of granularity. Furthermore, the approach makes the impact of different design parameters on the performance explicit so it provides invaluable insight into NoC design. As a result, the proposed approach can be used as a powerful design and optimization tool. Experimental results demonstrate the accuracy and efficiency of the analysis on real and synthetic benchmarks.

Mohmed Bakhouya et all[5] presented, a Network Calculus-based methodology to evaluate on-chip interconnects in terms of performance (i.e., latency, communication load, throughput) and cost metrics (i.e., energy consumption and area requirements) based on a given traffic pattern. The main objective is to illustrate the practical use of the Network Calculus approach to analytically evaluating on-chip interconnects. The 2D regular Mesh, Spidergon, and WK on-chip interconnect architectures are compared and evaluated using a given traffic pattern. The results show that this approach can provide the designer with initial insight on on-chip interconnects and the relationship between application traffic and performance. The results show that WKRecursive outperforms the 2D Mesh and Spidergon on-chip interconnects in all considered metrics.

Erno Salminen et all[6] presented a background, classification, and requirements for NoC benchmarking. It shortly introduced Transaction Generator that uses communication profiles that are easy to generate, fast to simulate, and accurate enough in NoC benchmarking. Furthermore, they have generated a parameterizable set of synthetic and real application models. The following tasks are to generate new benchmarks, to evaluate and report the performance of existing Network-on-Chips, and prepare the on-line distribution of the benchmark set.

Ahmed Ben Achballah and Slim Ben Saoud [7] tried to focus on a subject concerning NoCs that somehow was not deeply studied in the literature. This paper presented the NoC concept and its importance in recent SoCs. Then It presented the tools dedicated to their development which includes the modeling, simulation and implementation processes. It stress again at the fact that this list is not exhaustive but can represent an important number of nowadays available NoC tools. Meanwhile, when they are writing this manuscript some other tools emerged.

El Sayed M. Saad et all [8] proposed, a performance and power network on chip simulator (PPNOCS) based on SystemC. As demonstrated, PPNOCS is a general NoC simulation and verification platform with high

extensibility. Using PPNOCS, the impact of various architectural level parameters of the on-chip interconnection network elements on its performance and power can be explored. Owing to the general NoC node structure and modularization modeling, developers can develop their own routing algorithm and network topology in such a way that they can use either traffic patterns provided by PPNOCS or their own traffic pattern. Then, the simulation and design verification can be applied. By going through simulation experiments using five classic routing algorithms, the practical usage of PPNOCS is verified. Also, the impact of different traffic patterns, routing algorithms, virtual channel configurations, and packet length on the network performance and power is evaluated. As shown, PPNOCS provided a fast and convenient platform for researching and verification of NoC architecture and routing algorithm.

E. Salminen[9] presented the motivation, basic concepts, and requirements for benchmarking a Network-onChip (NoC). Currently there is practically no benchmark sets for NoC or the presented tools do not meet the requirements. The presented benchmarking method utilizes traffic generator with a dataflow models of the applications. Combined with transaction-level NoC, the abstract application model allows approximately 200x speedup and on average 10% error in estimated runtime w.r.t. cycle-accurate HW/SW co-simulation without exposing the exact internal functionality of the application.

III. NOC BUILDING BLOCK

An on-chip network can be designed by breaking it down into its various building blocks; namely, its topology, flow control, routing, link architecture, and router microarchitecture.

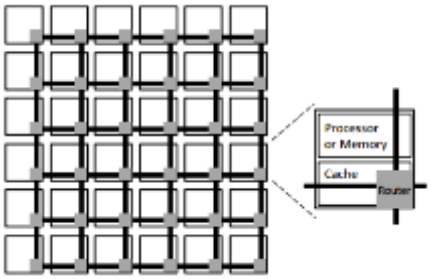

Figure 1.2 NoC building blocks

Topology: An NoC is made up of router nodes and channels. The logic connections between the network□s nodes and channels are determined by the network topology. Figure 1.2 shows an NoC with a 6x6 mesh topology.

Routing: The routing algorithm determines the path that a message takes through the network to reach its destination. The ability of a routing algorithm to balance load directly impacts the performance of the network.

Switching: Switching mechanism determines the way in which a network allocates resources to messages as they travel through the network. The switching mechanism allocates and de-allocates buffers and channel bandwidth to the packets that wait for them. While it is possible to allocate resources to packets in their entirety (this is done using store-and-forward and virtual cut-through switching), it is impractical to implement it in the NoCs because of the large buffer resources required. The most common method for on-chip networks is to handle flow control at the flit level. Allocating buffers and channel bandwidth on the smaller granularity of flits, as opposed to entire packets, makes it possible to design routers that have smaller buffers.

Router microarchitecture: The following components comprise a generic router microarchitecture: router state, input buffers, allocators, routing logic, and a crossbar (or switch). It is common to pipeline router functionality in order to improve throughput. The main contributor to communication latency is the delay in the on-chip network through each individual router. Because of this, researchers have made significant efforts to reduce router pipeline stages and improve throughput.

Link architecture: All on-chip network prototypes to date have utilized conventional pipelined wires and full-swing logic. Pipelined wires utilize repeaters in order to increase signal reach, but studies are underway to identify alternative link architectures, such as optical networks.

IV. NOC EVALUATIONS PARAMETERS

The important parameters of networks are latency, throughput, injection rate, and hop counts etc. In this paper most popular topologies□ performance parameters are discussed. The comparative evaluation of topologies will help to explore and understand various topologies in detail which will be helpful in further developing new topologies for NoC. Along with these parameters, there are some synthetic parameters used in simulation are like, traffic pattern and injection rate etc.

Traffic pattern: It is the spatial distribution of messages in the network, these message distributions gives fraction of traffic sent from source to destination, and it is used to evaluate interconnection network. Some examples are like random traffic, permutation traffic in which all the source convey all its traffic to only one destination.

Injection Rate: It is defined as average number of packet injected per cycle.

The metric used for measuring the NoC performance is saturation throughput and zero-load latency. Saturation throughput is defined as the network throughput at which the first channel saturates and zero-load latency represents a lower bound on the network latency. The performance of NoC mainly depends on few parameters which are given below:

Throughput: It is defined as data rate in bits per second at input port, it depends on parameters like routing, flow control and on topology. It measures how fast the message can pass through NoC. It can be calculated as:

$$TP = \frac{(M_{CP})*L}{H*t} \qquad (1.1)$$

where, MCP = number of message completed, L = message length, H = number of IP blocks and t = total time

Latency: Time requisite for a packet to navigate the network, time taken by the head-packet to arrive at the input port to the time taken by tail-packet to exit the output port. The average latency without any contention (TCL) starting from source S to final destination D depends on a various network parameters, which includes: the average hop count (H) from S to D and router delay (tr), which incorporate the latency due to routing; the average channel travel time (TC); serialization latency (TSL) and the length of packet (L) and bandwidth of channel (b). It can be estimated as:

$$T_{CL} = H \times t_r + T_C + T_{SL} \qquad (1.2)$$

Hop counts: The distance between nodes considered as the average number of channels and nodes a message must navigate from source node to destination node. The overall average hop count for all sources and destinations, called as average minimum hop count of network Havg , is defined as:

$$H_{avg} = \frac{1}{N^2} \sum s, d \in H(s, d) \qquad (1.3)$$

Where N=total number of nodes in network, H(s,d)=hop count of minimal path between s and d .

Path diversity: A property of network which has multiple paths between two nodes, this gives robustness to the network.

V. ROUTING ALGORITHM

The Routing algorithms define the path taken by a packet between source and target switches. They must prevent deadlock, livelock, and starvation situations. Deadlock may be defined as a cyclic dependency among nodes requiring access to a set of resources, so that no forward progress can be made, no matter what sequence of events happens. Livelock refers to packets circulating the network without ever making any progress towards their destination. Starvation happens when a packet in a buffer requests an output channel, being blocked because the output channel is always allocated to another packet.

Routing algorithms can be classified according to the three different criteria:

(i) where the routing decisions are taken;

(ii) how a path is defined, and

(iii) the path length.

According to where routing decisions are taken, it is possible to classify the routing in source and distributed routing. In source routing, the whole path is decided at the source switch, while in distributed routing each switch receives a packet and defines the direction to send it. In source routing, the header of the packet has to carry all the routing information, increasing the packet size. In distributed routing, the path can be chosen as a function of the network instantaneous traffic conditions. Distributed routing can also take into account faulty paths, resulting in fault tolerant algorithms. Depending how a path is defined, routing can be classified as deterministic or adaptive. In deterministic routing, the path is completely specified from the relative position of source and target addresses. In adaptive routing, the path is a function of the network instantaneous traffic. Adaptive routing increases the number of possible paths usable by a packet to arrive to its destination. However, deadlock and livelock situations can happen in fully adaptive algorithms, which limit its usage. Regarding the path length criterion, routing can be minimal or nonminimal. Minimal routing algorithms guarantee shortest paths between source and target addresses. In nonminimal routing, the packet can follow any available path between source and

target. Nonminimal routing offers great flexibility in terms of possible paths, but can lead to livelock situations and increase the latency to deliver the packet.

Deterministic Routing: The Dimension Order Routing is one kind of deterministic routing algorithms, such as XY routing algorithm for 2D-mesh. In this algorithm, the data packet is routed firstly along the X-dimension and then along the Y-dimension until the packet reaches its final destination. The path between the source and destination used by this algorithm is one of the shortest ones but always the same. XY routing has low latency at low network traffic due to its static, but the performance decreases quickly when the network becomes congested for lacking path diversity. XY routing algorithm performs better than other routing algorithm under uniform traffic pattern, but under non-uniform traffic pattern, XY routing blindly maintains the unevenness of the non-uniform traffic, just as it maintains the evenness for the uniform traffic, the load in the center of a network is much higher rather than total average and this leads to hot spot in the center of network. Another disadvantage of XY algorithm is that it cannot handle with faulty nodes and regions. If a faulty node or regions (area in the networks having a size larger than a tile) is placed on the path between the source and destination, the packet will remain blocked in one of the switches. However, XY routing has its own advantages, the routing algorithm is simple and can be implemented easily, and its router architecture is very simple and has lower hardware overhead than adaptive router. Then XY routing easily supports in-order end-to-end packet delivery. Moreover XY routing can easily avoid deadlock and livelock. Therefore, it is not surprising that designers would like to use deterministic routing algorithms in the NoCs which suffer from limited silicon resources.

Partially Adaptive Routing: Examples of the partially-adaptive routing algorithms are the turn model types. In the algorithms based on the turn model, three partially adaptive routing algorithms, namely west-first, north-last, and negative-first, were presented for two-dimensional meshes. The basic idea of turn model is to prohibit the minimum number of turns that break all of the cycles so that deadlock can be avoided. Unfortunately, the degree of adaptiveness provided by the turn model is highly uneven, at least half of the source destination pairs are restricted to having only one minimal path, while full adaptiveness is provided for the rest of the pairs. Such uneven adaptiveness not only causes unfairness but also curtails the ability of the model in alleviating traffic congestion problem. Performance of the network communication may be affected as a result. An improvement routing algorithm namely Odd-Even(OE) based on turn model is proposed, OE routing algorithm is a sort of distributed partially adaptive routing algorithms, which provides more even routing adaptiveness . by comparing with XY routing,OE routing has a lower average latency and has a higher throughout, also, when the networks has relate high injection rate, OE routing can balance load better due to its path diversity. However, as well as other adaptive routing, packets may be delivered by different paths, this may cause packets to arrive out-of-order at receiver. Thus, some control logic should be added to guarantee that packets can be received in order at destination.

Fully Adaptive Routing: In fully adaptive routing, each physical channel of the network is shared between k virtual channels ($k > 1$). Virtual channels in turn are divided into two classes namely deterministic class and adaptive class. Consequently, the network is divided into deterministic and adaptive virtual networks. Packets in the adaptive virtual network are routed without any restriction i.e., packets can choose every virtual channel which makes them closer to destination nodes. In the deterministic virtual network on the other hand, packets are routed according to a deterministic routing algorithm. In the case of a deadlock occurrence between packets traversing in the adaptive virtual network, the deadlock handling mechanism selects one of the engaged packets and releases to break the group dependency. The selected packet then will be routed in the deterministic virtual network until the deadlock is completely resolved. Fully adaptive routing algorithms have lower average packet latency and higher throughout. However, it has the same problems as partially routing and needs more energy dissipation as compared to the deterministic routings, the manner to prevent deadlock and livelock is very complex.

CONCLUSIONS

Network on Chip (NoC) is a new paradigm for System on Chip (SoC) design. Increasing integration produces a situation where bus structure, which is commonly used in SoC, becomes blocked and increased capacitance poses physical problems. In this paper we discussed various performance parameters used to evaluate NoC viz. Traffic pattern, Injection Rate, Throughput, Latency, Hop counts and Path diversity. The Routing algorithms define the path taken by a packet between source and target switches. We also discussed various routing algorithms and their performance impact. According to where routing decisions are taken, it is possible to classify the routing in source and distributed routing. Depending how a path is defined, routing can be classified as deterministic or adaptive. Regarding the path length criterion, routing can be minimal or nonminimal. Minimal routing algorithms guarantee shortest paths between source and target addresses. In nonminimal routing, the packet can follow any available path between source and target. Nonminimal routing offers great flexibility in terms of possible paths, but can lead to livelock situations and increase the latency to deliver the packet.

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