(IJIRSE) International Journal of Innovative Research in Science & Engineering
ISSN (Online) 2347-3207

An Efficient Carry Select Adder

with Reduced Area Application

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***Abstract*: - Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. From the structure of the CSLA, it is clear that there is scope for reducing the area and power consumption in the CSLA. This work uses a simple and efficient gate-level modification to significantly reduce the area and power of the CSLA. Based on this modification 8-, 16-, 32-, 64- and 128-bit square-root CSLA (SQRT CSLA) architecture have been developed and compared with the regular SQRT CSLA architecture. The proposed design has reduced area and power as compared with the regular SQRT CSLA with only a slight increase in the delay.**

Keywords- VERILOG HDL, Xilinx 14.3.

I. INTRODUCTION

DESIGN of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum [1]. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input 0 and carry input 1, then the final sum and carry are selected by the multiplexers (mux).

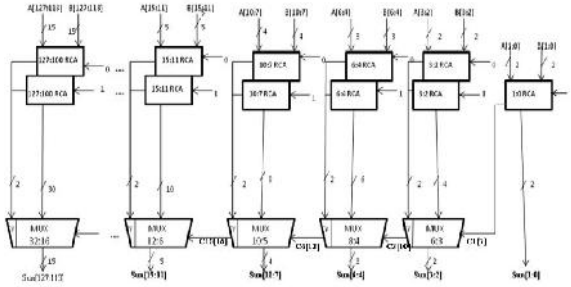
II. REGULAR METHOD

A. Description

A 16-bit carry select adder can be developed in two different sizes namely uniform block size and variable block size. Similarly a 32, 64 and 128-bit can also be developed in two modes of different block sizes. Ripple-carry adders are the simplest and most compact full adders, but their performance is limited by a carry that must propagate from the least-significant bit to the most-significant bit. The various 16, 32, and 64-bit CSLA can also be developed by using ripple carry adders. The speed of a carry-select adder can be improved up to 40% to 90%, by performing the additions in parallel, and reducing the maximum carry delay. It includes many ripple carry adders of variable sizes which are divided into groups. Group 0 contains 2-bit RCA which contains only one ripple carry adder which adds the input bits and the input carry and results to sum [1:0] and the carry out. The carry out of the Group 0 which acts as the selection input to mux which is in group 1, selects the result from the corresponding RCA (Cin=0) or RCA (Cin=1). Similarly the remaining groups will be selected depending on the Cout from the previous groups.

In Regular CSLA, there is only one RCA to perform the addition of the least significant bits [1:0]. The remaining bits (other than LSBs), the addition is performed by using two RCAs corresponding to the one assuming a carry-in of 0, the other a carry-in of 1 within a group. In a group, there are two RCAs that receives the same data inputs.but different Cin. The upper adder has a carry-in of 0, the lower adder a carry-in of 1. The actual Cin from the preceding sector selects one of the two RCAs. That is, as shown in the Fig.4, if the carry-in is 0, the sum and carry-out of the upper RCA is selected, and if the carry-in is 1, the sum and carry-out of the lower RCA is selected.

B. Regular CSLA architecture



C. Basic adder block

In this we calculate and explain the delay & area using the theoretical approach and show how the delay and area effect the total implementation. The AND, OR, and Inverter (AOI) implementation of an XOR gate is shown in Fig. 1. The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter, each having delay equal to 1 unit and area equal to 1 unit. The area evaluation is done by counting the total number of AOI gates required for each logic block. Based on this approach, the blocks of 2:1 mux, Half Adder (HA), and FA are evaluated and listed in Table I.

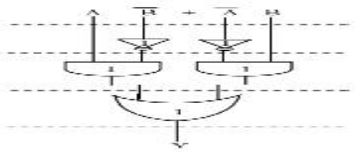


Fig.1: Delay and Area Evaluation of XOR.

Adder Blocks	Delay	Area
XOR	3	5
2:1 MUX	3	4
Half Adder	3	6
Full Adder	6	13

TABLE 1: Delay and Area Evaluation of CSLA.

D. Regular CSLA area evaluation

The structure of the 16-b regular SQRT CSLA is shown in Fig. 4. It has five groups of different size RCA. The delay and area evaluation of each group are shown in Fig. 5, The steps leading to the evaluation are as follows

1) The group2 [see Fig. 5(a)] has two sets of 2-b RCA. Based on the consideration of delay values of Table I, the arrival time of selection input c1[time(t)=7] of 6:3 mux is earlier than s3[time(t)=8] and later than s2[t=6]. Thus, sum3[t=11] is summation of s3 and mux[t=3] and sum2[t=10] is summation of c1 and mux.

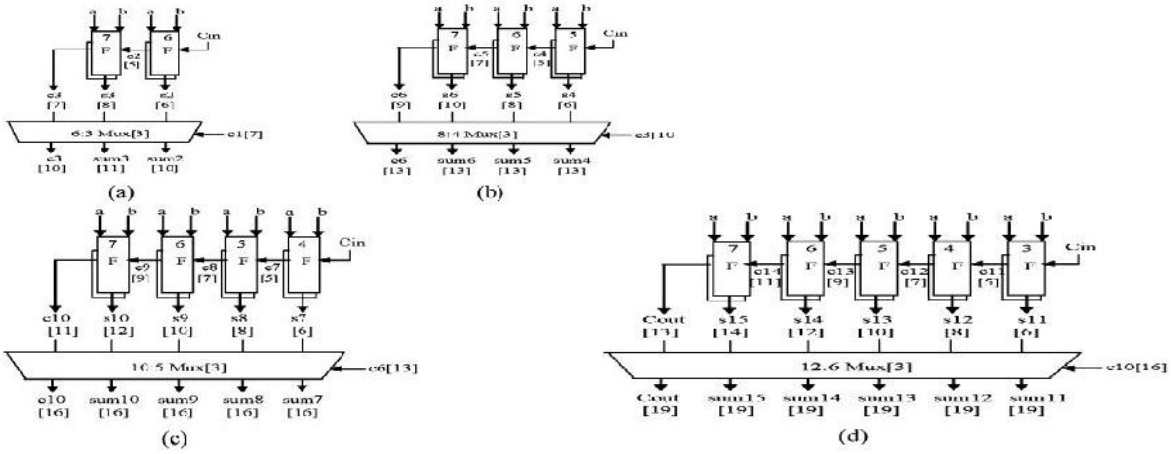


Fig. 5. Delay and area evaluation of regular SQRT CSLA: (a) group2, (b)group3, (c) group4, and (d) group5. F is a Full Adder

2) Except for group2, the arrival time of mux selection input is always greater than the arrival time of data outputs from the RCA s. Thus, the delay of group3 to group5 is determined, respectively as follows:

$$\{c6, \text{sum}[6:4]\} = c3[t=10] + \text{mux}$$
$$\{c10, \text{sum}[10:7]\} = c6[t=13] + \text{mux}$$
$$\{\text{cout}, \text{sum}[15:11]\} = c10[t=16] + \text{mux}.$$

3) The one set of 2-b RCA in group2 has 2 FA for cin=1 and the other set has 1 FA and 1 HA for cin=0 . Based on the area count of Table I, the total number of gate counts in group2 is determined as follows:

$$\text{Gate count} = 57\ (\text{FA} + \text{HA} + \text{Mux})$$
$$\text{FA} = 39(3 * 13)$$
$$\text{HA} = 6(1 * 6)$$
$$\text{Mux} = 12(3 * 4).$$

III. PROPOSED METHOD

A. Description

This architecture is similar to regular 128-bit SQRT CSLA, the only change is that, we replace RCA with Cin=1 among the two available RCAs in a group with a BEC. This BEC has a feature that it can perform the similar operation as that of the replaced RCA with Cin=1. Fig. 5 shows the Modified block diagram of 128-bit SQRT CSLA. The number of bits required for BEC logic is 1 bit more than the RCA bits. The modified block diagram is also divided into various groups of variable sizes of bits with each group having the ripple carry adders, BEC and corresponding mux. Group 0 contain one RCA only which is having input of lower significant bit and carry in bit and produces result of sum [1:0] and carry out which is acting as mux selection line for the next group, similarly the procedure continues for higher groups but they includes BEC logic instead of RCA with Cin=1.Based on the consideration of delay values, the arrival time of selection input C1 of 6:3 mux is earlier than the sum of RCA and BEC. For remaining groups the selection input arrival is later than the RCA and BEC.

B. Modified CSLA architecture

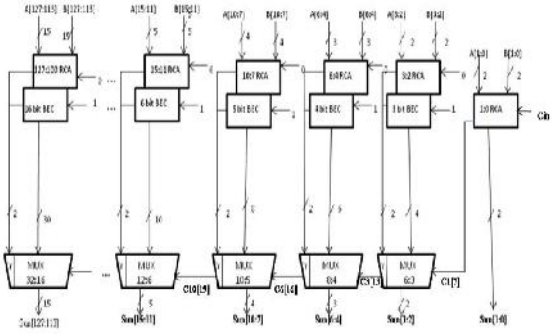


Fig. 5. Modified 128-bit SQRT CSLA. The parallel RCA with Cin = 1 is replaced with BEC.

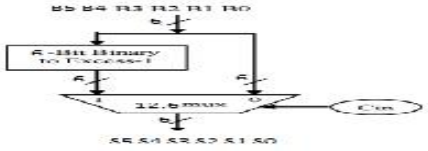


Fig. 2: 6-bit BEC with 12:6 mux.

Fig. 2 shows the basic 6-bit addition operation which includes 6-bit data, a 6-bit BEC logic and 12:6 mux. The addition operation is performed for Cin=0 and for Cin=1.For Cin=0 the addition is performed using ripple carry adder and for Cin=1 the operation is performed using 6-bit BEC (replacing the RCA for Cin=1). The resultant is selected based on Carry in signal from the previous group. The total delay depends on mux delay and Cin signal from previous group.

C. Binary to excess-1 converter(bec)

The basic work is to use Binary to Excess-1 Converter (BEC) in the regular CSLA to achieve lower area and increased speed of operation. This logic is replaced in RCA with Cin=1. To replace the n-bit RCA, n+ 1 bit BEC logic is required. The structure and the function table of a 6-bit BEC are shown in Figure.3 and Table .2

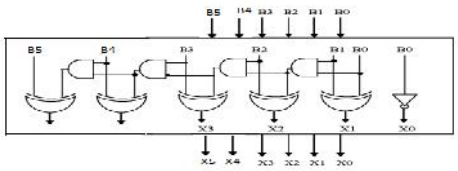


Fig. 3: 6-bit BEC Structure.

B[5:0]	X[5:0]
000000	000001
000001	000010
.	.
.	.
111111	000000

TABLE 2: Function Table Of The 6-bit BEC

D. Modified CSLA area evaluation

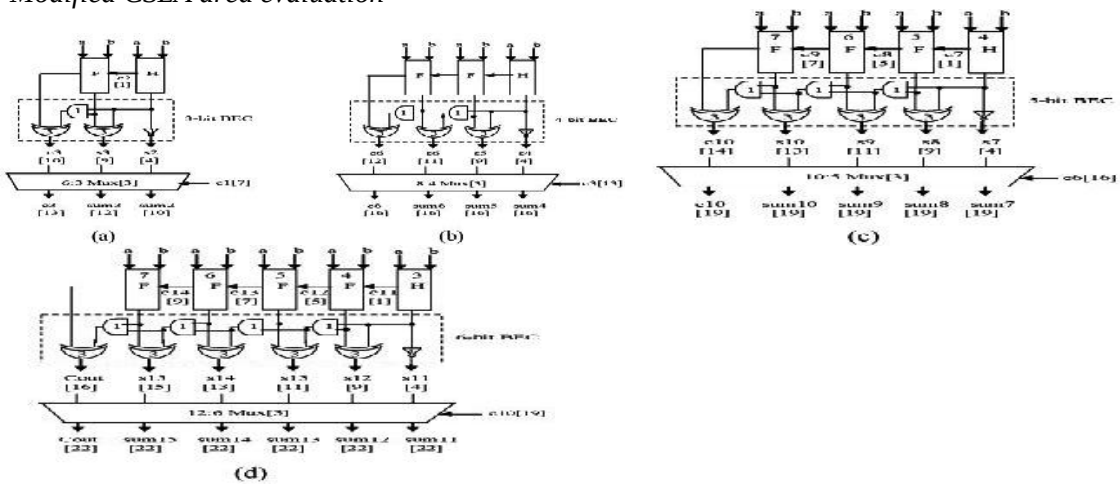


Fig. 7. Delay and area evaluation of modified SQRT CSLA: (a) group2, (b) group3, (c) group4, and (d) group5.

The structure of the proposed 128-bit SQRT CSLA using BEC for RCA with cin=1 to optimize the area and power is shown in Fig. 6. We again split the structure into five groups. The delay and area estimation of each group are shown in Fig. 7. The steps leading to the evaluation are given here.

1) The group2 [see Fig. 7(a)] has one 2-b RCA which has 1 FA and 1 HA for cin=0. Instead of another 2-b RCA with cin=1 a 3-b BEC is used which adds one to the output from 2-b RCA.

2) For the remaining group s the arrival time of mux selection input is always greater than the arrival time of data inputs from the BEC s. Thus, the delay of the remaining groups depends on the arrival time of mux selection input and the mux delay.

3) The area count of group2 and Gate count comparision determined as follows:

$$\text{Gate count} = 43\,(\text{FA} + \text{HA} + \text{Mux} + \text{BEC})$$
$$\text{FA} = 13(1*13)$$
$$\text{HA} = 6(1*6)$$
$$\text{AND} = 1$$
$$\text{NOT} = 1$$
$$\text{XOR} = 10(2*5)$$
$$\text{Mux} = 12(3*4).$$

GROUP	RREGULAR	MODIFIED
GROUP 2	57	43
GROUP 3	84	61
GROUP 4	117	84
GROUP 5	147	107

Gate count comparision

IV. CONCLUSION

The reduced number of gates of this work offers the great advantage in the reduction of area and also the total power. The modified CSLA architecture is therefore, low area, low power, simple and efficient for VLSI hardware implementation. It would be interesting to test the design of the modified 128-b SQRT CSLA.

ACKNOWLEDGMENT

The authors would like to thank M.Manjula, and A.Charan of the VLSI Division, MRRITS, Udayagiri, India, for their contributions to this work

REFERENCES

[1] O. J. Bedrij, Carry-Select Adder , IRE transactions on Electronics Computers, vol.EC-11, pp. 340-346, June1962. .
[2] T.Y. Ceiang and M.-J. Hsiao, Carry-Select Adder using single Ripple-Carry Adder , Electronics letters, vol.34, pp.2101-2103, October 1998.
[3] Y. Kim and L.-S. Kim, 64-bit carry-select adder with reduced area , Electronics Letters, vol.37, issue 10, pp.614-615, May 2001.
[4] J. M. Rabaey, Digital Integrated Circuits- A Design Perspective , New Jersey, Prentice-Hall, 2001.. Adder , Electronics letters, vol.34, pp.2101-2103, October 1998.
[5] Y. He, C. H. Chang, and J. Gu, An Area Efficient 64-bit Square root carry select adder for Low power Applications, in Proc IEEE Int. Symp. Circuits Syst.2005, vol. 4, pp. 4082-4085.
[6] Akhilesh Tyagi, A Reduced Area Scheme for Carry-Select Adders , IEEE International Conference on Computer design, pp.255-258, Sept 1990.

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