Rearranged SVPWM Algorithm For Neutral Point Clamped 3-Level Inverter Encouraged DTC-IM Drive

Yelem Srikanth

M.Tech Student, Dept of EEE, Rajeev Gandhi Memorial College of Engineering &Technology,

Nandyal, Andhra Pradesh, India

(email:sri261eee@gmail.com)

Abstract: In this paper, an Rearranged space vector pulse width modulation (SVPWM) strategy has been created for three stage three-level voltage source inverter bolstered to direct torque controlled (DTC) induction engine drive. The space vector outline of three-level inverter is streamlined into two-level inverter. So the choice of exchanging arrangements is done as conventional two-level SVPWM system. Where in conventional direct torque control (CDTC), the stator flux and torque are straight forwardly controlled by the determination of ideal switching modes. The choice is made to limit the flux and torque slips in comparing hysteresis groups. Not with standing its quick torque response, it has more flux, torque and current swells in steady state. To beat the swells in steady state, a space vector based pulse width modulation (SVPWM) technique is proposed in this paper. The proposed SVPWM system reduces the computational burden and decreases the total harmonic distortion compared with 2-level one and the conventional one too. To fortify the voice simulation is completed and the relating results are presented.

Keywords-: Rearranged SVPWM, DTC.

I. INRODUCTION

The pulse width modulated voltage source inverters (PWM-VSI) sustained variable rate induction engine drives have increased more significance in numerous mechanical applications. The development of the field orinted control (FOC) acquired a renaissance the field of superior drives. The FOC calculation controls the induction engine like that of an independently energized dc motor[1]. In any case, the intricacy included in FOC calculation is all the more because of reference frame changes. To reduce the complexity in the calculation and to accomplish decoupled control, another torque control methodology has proposed in [2]. A definite examination in the middle of FOC and DTC has been displayed in [3] and reasoned that DTC gives great dynamic reaction when compared with FOC. In spite of the fact that DTC gives great dyanamic execution, it gives extensive steady state swells in torque, flux and currents. To reduce the swells, discrete space vector modulation (DSVM) calculation has proposed in [4]. In any case, the established DTC and DSVM based DTC display variable exchanging frequency operation of the inverter. To reduce the swells further, these days, the multilevel inverters are getting to be mainstream A diode clamped three-level inverter has proposed in [5]. Three-level inverter based DTC has proposed in [6], which utilizes the changing tables to create the gating pulses of the inverter. To accomplish the constant exchanging frequency operation and to diminish the harmonic distortion different pulse width balance calculations have been produced. An itemized study on different PWM calculations is given in [7]. Among the different PWM calculations, the space vector pulse width modulation (SVPWM) is famous because of its various favorable advantages [8]. To accomplish the consistent exchanging frequency operation, SVPWM calculation is utilized for DTC as a part of

[9]. As the quantity of levels increments in a multilevel inverter, the complexity involved in the SVPWM calculation likewise increments. To decrease the complexity , an Rearranged SVPWM calculation has been proposed for three-level inverter in [10]. This paper introduces a Rearranged SVPWM calculation for three-level inverter fed direct torque controlled induction engine drives. The proposed calculation utilizes the idea of SVPWM calculation which is utilized for two-level inverter.

II. CONVENTIONAL DTC

The block diagram representation of CDTC is indicated in Fig 1. The stator currents and DC bus voltage are examined at each testing inverter of time. Speed, torque, stator flux and flux angel are assessed in the adaptive engine model show by considering voltages, currents to the drive. The evaluated torque and flux are contrasted and their comparing hysteresis comparators separately. The quantity of division where the stator flux space vector is found and the yields of hysteresis comparators are encouraged to optimal changing table to choose a proper voltage vectors. At that point this voltage space vector is connected to inverter.

III. SPACE VECTOR PWM ALGORITHM

Among these voltage vectors, V1 to V6 vectors are known as dynamic voltage vectors or dynamic states and the staying two vectors are known as zero states or zero voltage vectors. The reference voltage space vector or test, which is as indicated in Fig.2 represents to the relating to the wanted estimation of the basic segments for the yield phase voltages. In the space vector approach this can be built in a normal sense. Vref is inspected at equivalent interval of time, Ts reffered to as examining time period. Distinctive voltage vectors that can be created by the inverter are connected over diverse time spans with in an examining time period such that the normal vector delivered over the inspecting time period is equivalent to the examined estimation of the Vref , both regarding magnitude and angle. It has been set up that the vectors to be utilized to produce any example are the zero voltage vectors and the two dynamic voltage vectors framing the limit of the area in which the sample lies. As every one of the six sectors are symmetrical, the exchange is restricted to the first division just. For the obliged reference voltage vector, the dynamic and zero voltage vectors times can be ascertained as in (1), (2) and (3).

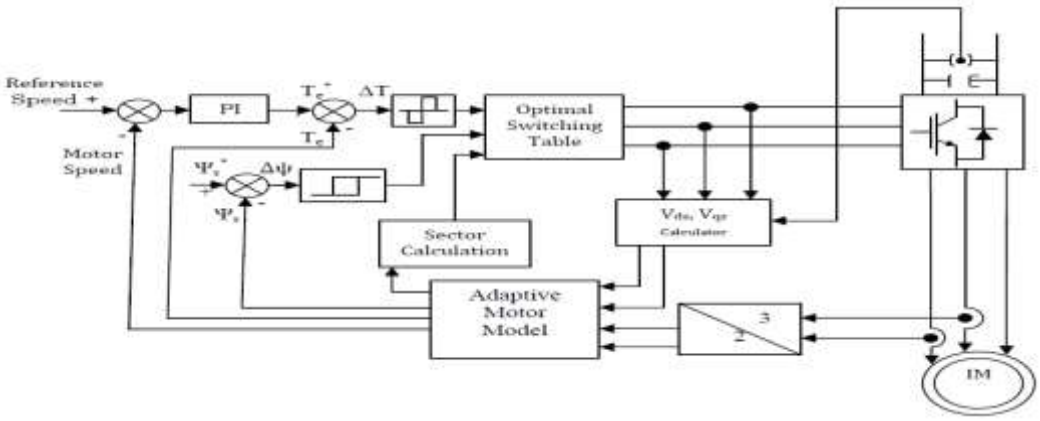

Fig. 1 Block Diagram of CDTC

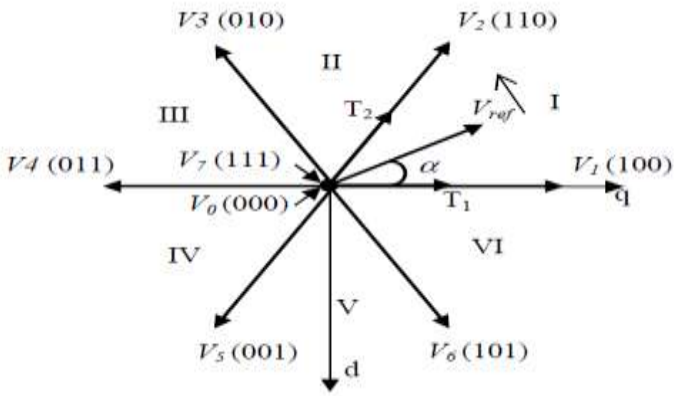

Fig. 2 Possible voltage space vectors

$$T_1 = \frac{2\sqrt{3}}{\pi} M_i \sin(60° - \alpha) T_s \quad (1)$$

$$T_2 = \frac{2\sqrt{3}}{\pi} M_i \sin(\alpha) T_s \quad (2)$$

$$T_z = T_s - T_1 - T_2 \quad (3)$$

where M_i is the regulation record and characterized as in [7]. In the SVPWM calculation, the total zero voltage vector time is similarly partitioned between V0 and V7 and distributed symmetrically toward the begin and end of the every examining time period. Consequently, SVPWM utilizes 0127-7210 in division I, 0327-7230 in sector- II etc.

IV. Rearranged SVPWM Algorithm For Three-Level Inverter

A three level diode clamped inverter circuit outline is indicated in Fig.3. The space vectors connected with in the three level inverter on d-q plane are indicated in Fig.3. In SVPWM approach, the reference vector V_r is examined at consistent interval of time Ts. The tested reference vector is approximated by time averaging the closest three vectors V_x,V_y and V_z as

$$V_r T_s = V_x T_x + V_y T_y + V_z T_z \quad (4)$$

where Tx , Ty and Tz are the stay times of V_x,V_y, andV_z separately. The zero vectors are not present in all the sectors, where these are available in two level inverters. So as to rearrange the above comparisons, the space vector plane of three level inverter indicated in Fig.4 is subdivided into six parts each of 60° as demonstrated in Fig.5 every part S, S= 1,2… ,6 are consists of one pivot vector V_s and other six vectors of segment 1 is recreated in Fig.6 (a). The vectors of alternate parts are stage shown by $\pi/3$ radians. All the vectors connected with the given sector S are mapped to a situated of seven invented vectors with V_1 as pivot vector in centre as characterized by (5) - (8), and spoke to in Fig. 6(b)

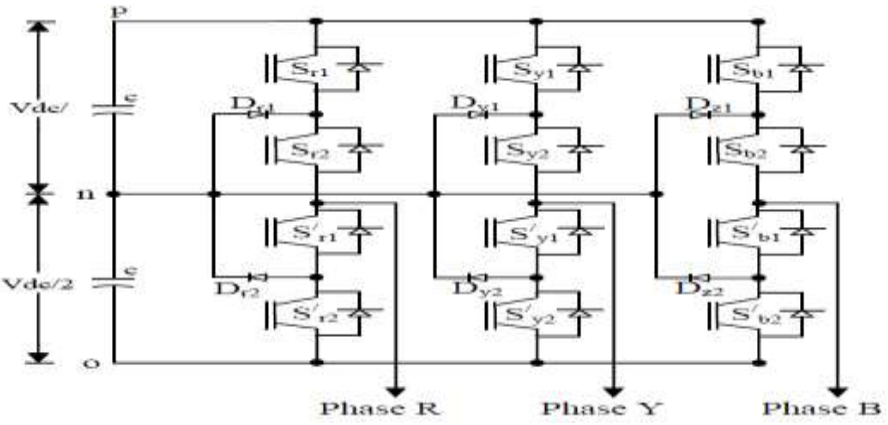

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Fig.3 circuit diagram of three level diode clamped inverter.

$$V_r^1 = V_r\, e^{j(s-1)\frac{\pi}{3}} - V_1 \quad (5)$$

$$V_x^1 = V_x\, e^{j(s-1)\frac{\pi}{3}} - V_1 \quad (6)$$

$$V_y^1 = V_y\, e^{j(s-1)\frac{\pi}{3}} - V_1 \quad (7)$$

$$V_z^1 = V_z\, e^{j(s-1)\frac{\pi}{3}} - V_1 \quad (8)$$

The vector V_z^1 shapes the origin and its magnitude is constantly zero and for a given segment this vector is like the zero vector of two level inverters. The three closest vectors can be distinguished as V_z^1,V_x^1 and V_y^1 as indicated in Fig.5 now the answer for (4) is like that of two level inverters,
As

$$V^1_{r\alpha}\, T_s = V^1_{x\alpha}\, T_s + V^1_{y\alpha}\, T_y \quad (9)$$

$$V^1_{r\beta}\, T_s = V^1_{x\beta}\, T_s + V^1_{y\beta}\, T_y \quad (10)$$

$$T_z = T_s - T_x - T_y \quad (11)$$

The proposed system requires just the figuring of V^1_r, subsequently calculation of three level is comparative and test as that of two level. The exchanging successions of conventional SVPWM are $V_{zx} - V_x - V_y - V_{zy}$ and the T_z interval is equally distributed between pivot vectors V_{zx} and V_{zy} . The state V_{zx} is signified as the state of V_z acquired by exchanging only one phase of the inverter stateV_x and state V_{zy} is characterized as the state of V_z which has obtained by exchanging one and only phase of the inverter state V_y . This infers that every phase is exchanged in any event ones in every testing time. During the state transmission one and only change must be exchanged. Also, in current state whatever is the last state that would be the starting state in next example needs to fulfill for least exchanging frequency operation.

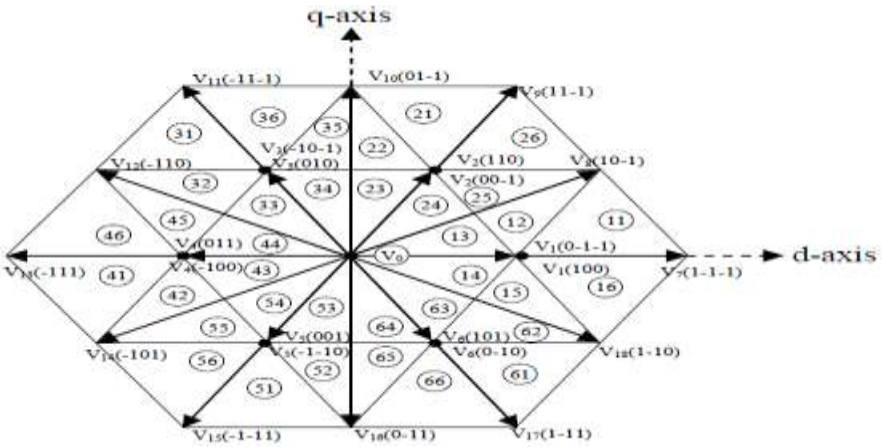


Fig.4 Space vector diagram of three-level inverter.

5. Rearranged SVPWM Algorithm For Three-Level Inverter

The square outline of proposed DTC is indicated in Fig.7. In every testing time period, the flux errors are to be minimized which could be brought about by ψ_s and ψ_s^* .And summation of genuine rotor speed ω_r and extra slip speed ω_{sl} will deliver the velocity of ψ_s^* .The suitable reference voltage space vectors delivered by reference voltage vector adding machine piece are

$$V_{ds}^{*} = R_s i_{ds} + (\Delta\psi_{ds}) / T_s \quad (12)$$

$$V_{qs}^{*} = R_s i_{qs} + (\Delta\psi_{qs}) / T_s \quad (13)$$

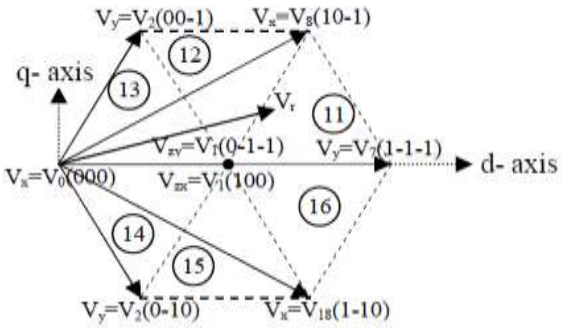
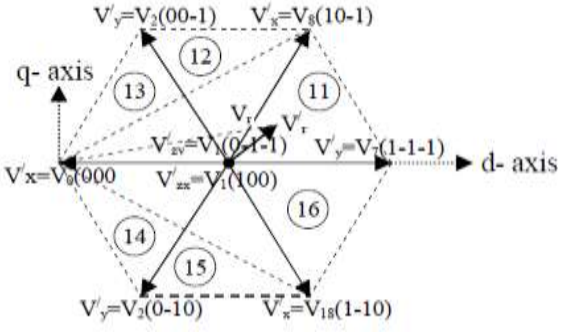


Fig. 5 (a) vectors of Sector 1



(b) Mapping of sector 1 to fictitious vector

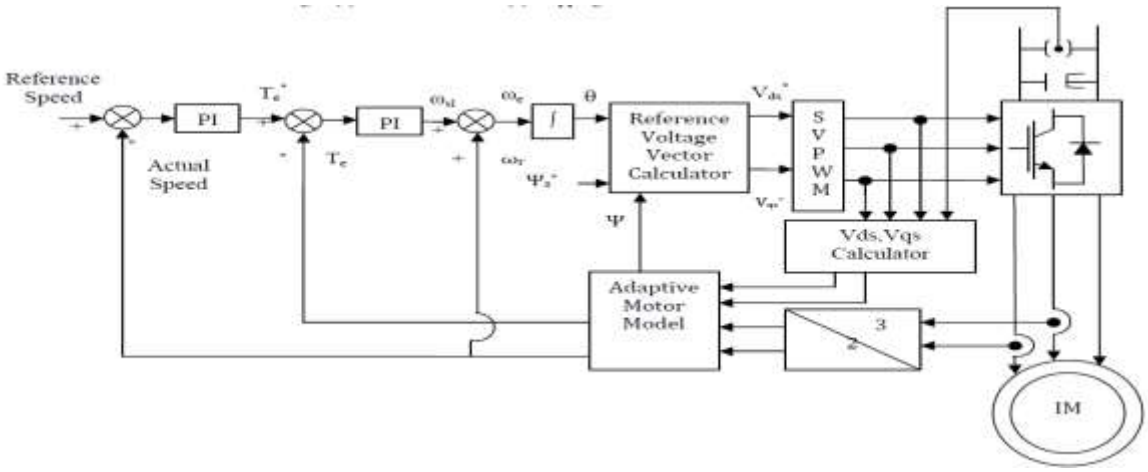


Fig.6 Block diagram of proposed DTC drive.

6. SIMULATOIN RESULTS

By using Matlab/Simulink, the advantage of SVPWM application as a numerical simulation has been carried out with fixed step size of 1μs in ode4 (runge-kutta) method. A 3-phase, 4 pole, 4kW, 1200rpm induction motor with parameters of R_s = 1.57Ω, R_r = 1.21Ω, L_s = L_r = 0.17H, L_m=0.165H and J = 0.089Kg.m2 are considered. The steady state plots of conventional DTC are shown in Fig.7-8. From which , it can be experiential that conventional DTC gives large steady state swells and more harmonic distortion. To reduce the swells, Rearranged SVPWM algorithm is used for 2-level inverter. The simulation results for Rearranged SVPWM algorithm based 2-level inverter fed DTC-IM drive are shown in Fig. 9 - Fig. 10. The simulation results of proposed Rearranged SVPWM algorithm based 3-level inverter fed DTC-IM drive are shown in Fig. 11 - Fig. 16.

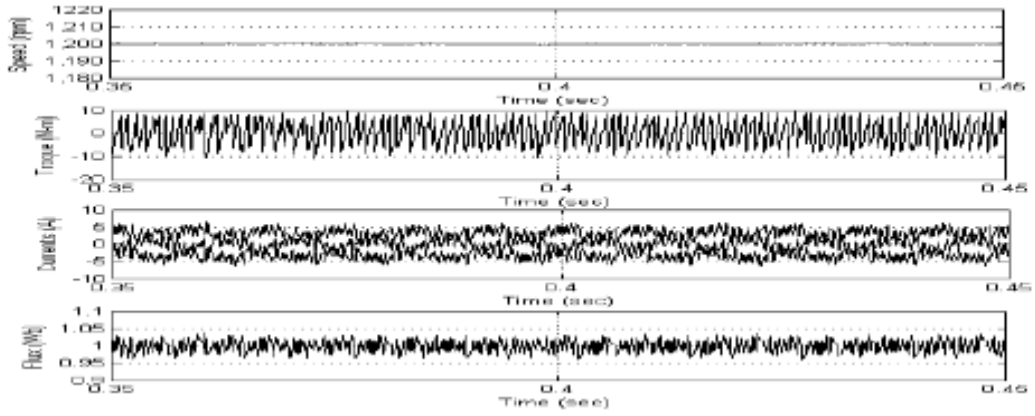


Fig.7 steady state plots of speed, torque, stator currents and stator flux for CDTC based IM drive at 1200 rpm.

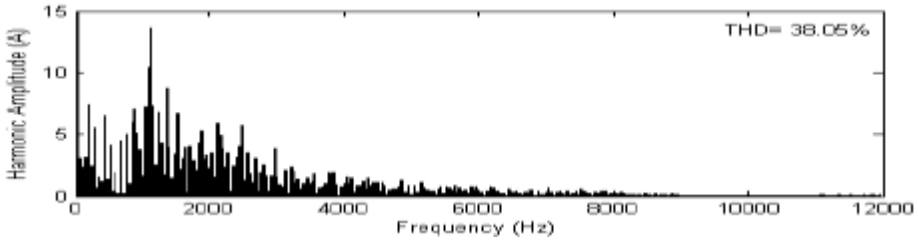


Fig 8 Harmonic Spectrum of stator current along with THD.

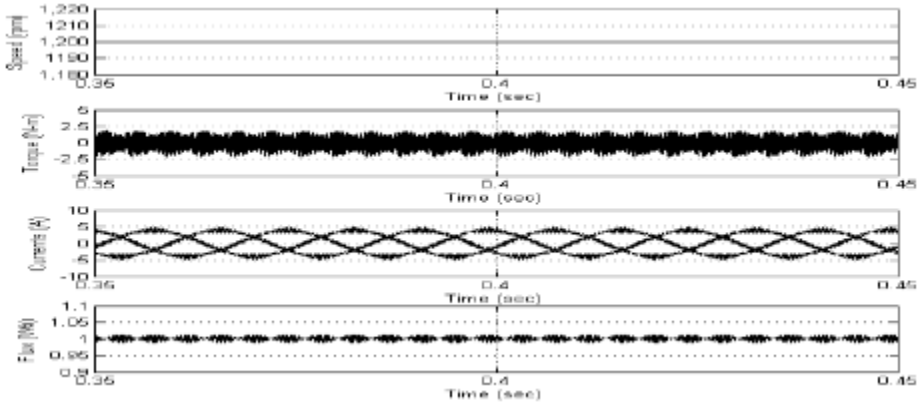


Fig. 9 Simulation results of 2-level SVPWM based DTC: steady-state plots at 1200 rpm.

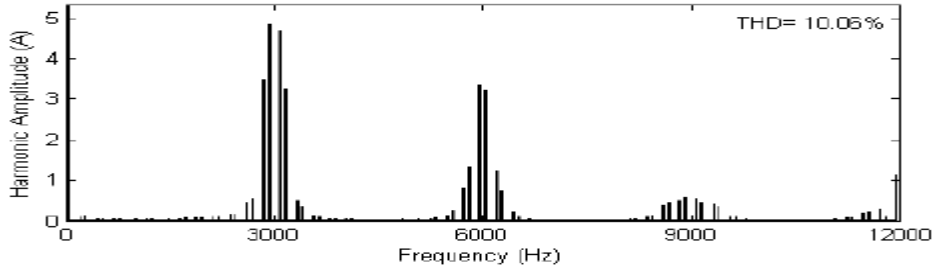


Fig. 10 Harmonic Spectrum of stator current along with THD for 2-Level SVPWM based DTC-IM drive.

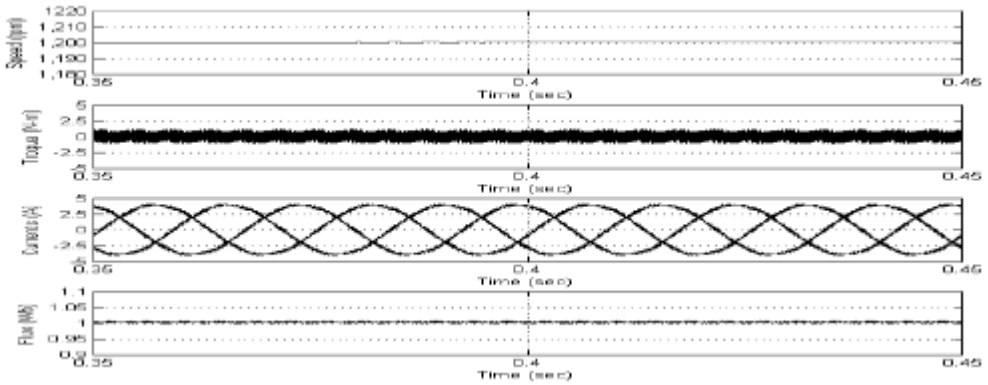


Fig. 11 Steady state plots of speed, torque, currents and flux for Rearranged SVPWM algorithm based 3-level inverter fed DTC-IM.

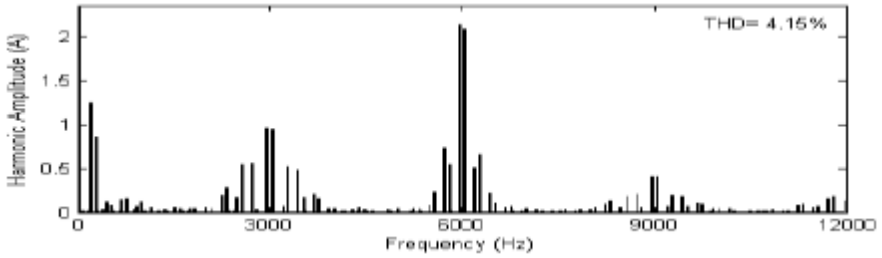


Fig. 12 Harmonic spectra of steady state line current for Rearranged SVPWM algorithm based 3-level inverter fed DTC-IM.

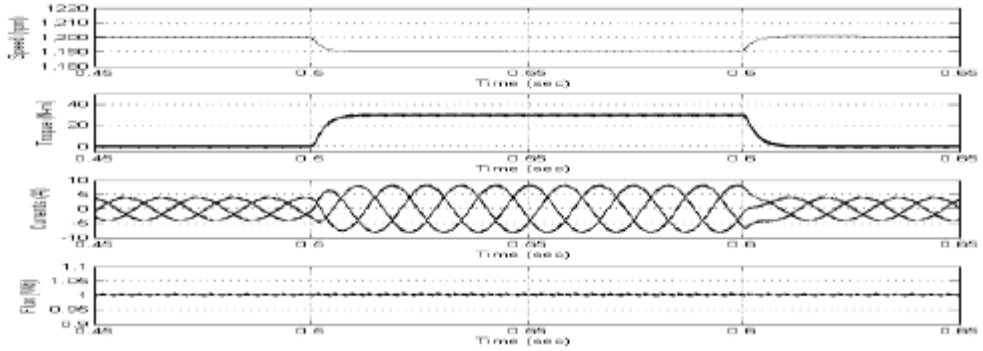


Fig. 13 transients during step change in load for Rearranged SVPWM algorithm based 3-level inverter fed DTC-IM: a 30 N-m load is applied at 0.5 sec.

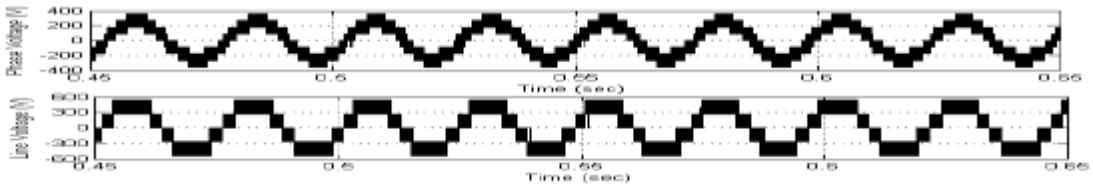


Fig. 14 Phase and line voltages during a step change in load for Rearranged SVPWM algorithm based 3-level inverter fed DTC-IM: a 30 N-m load is applied at 0.5 sec.

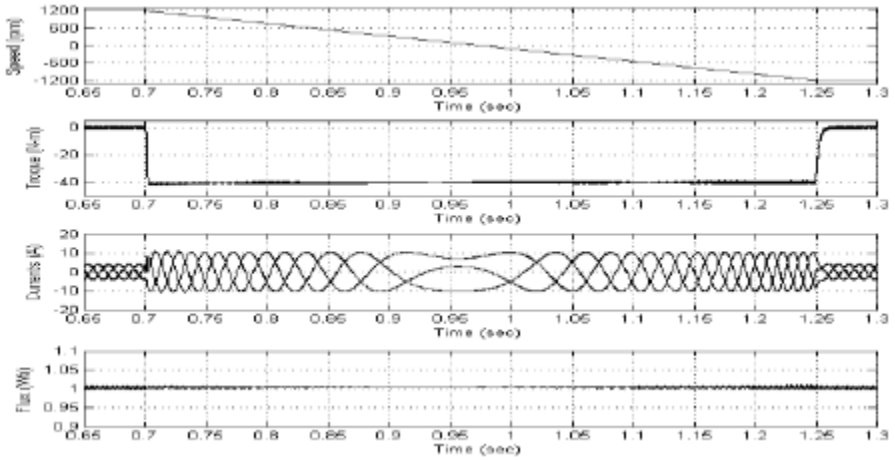


Fig.15 Transients in speed, torque, currents amd flux during speed reversal for Rearranged SVPWM algorithm based 3-level inverter fed DTC-IM

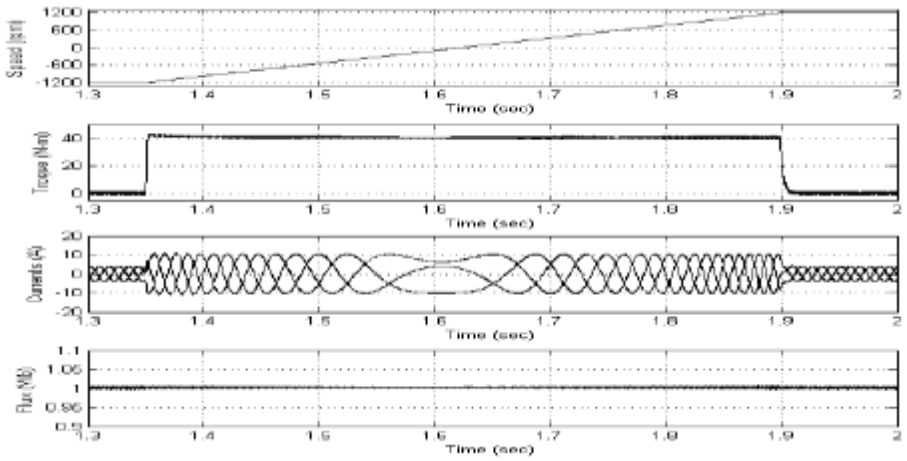


Fig. 16 Transients in speed, torque, currents and flux during speed reversal for Rearranged SVPWM algorithm based 3-level inverter fed DTC-IM (speed is changed from -1200 rpm to +1200 rpm at 1.35 s)

CONCLUSION

In this paper, a rearranged SVPWM calculation is introduced for three-stage three-level inverter encouraged DTC drive. The proposed calculation creates the changing heartbeats like a two-level inverter based SVPWM calculation. Along these lines, the proposed calculation diminishes the intricacy included in the current PWM calculations. To approve the proposed PWM calculation, numerical reproduction studies have been completed and results are exhibited. From the reproduction results, it can be inferred that the three-level inverter nourished DTC drive gives lessened relentless state swells and consonant mutilation.

FUTURE SCOPE

The present work can be implement in hardware for industrial applications. The proposed Rearranged SVPWM algorithm can be developed by using the artificial intelligent (AI) techniques.The present work can be extended to further level inverters. With an increase in the number of possible switching states, an improved performance can be measured in terms of THD and switching loss.

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